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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,739	LU ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-114* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-114* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/11/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-114 have been presented for examination based on the application filed on 8th February 2002.

Claim Rejections - 35 USC § 112 ¶1

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 1 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 dislcoses:

> "...utilizing the simulation results and the HDL code to determine which of the components in the circuit connection graph are active components, an active component being any component in the circuit connection graph having an active output signal, an active output signal being any output signal of any component in the circuit connection graph that obtains a state between the start time and the stop time in response to a state change of the at least a start signal according to an execution path of the HDL code;"

Specification discloses the rule table for an OR gate implementation to determine whether the active input is a required input (Table 1; [0038]). The third combination (C2=1, A2=1, B2=1) making the active input value (A2) a required input, contradicts the claimed language that the active output signal (C2) is a output signal of any component in the circuit connection graph that obtains a state between the start time and the stop time in response to a state change of the at least a start signal (A2

here). The change in A2 did not cause the change in the state of the output signal, hence the claimed claim is not enabled for the OR gate implementation as disclosed in the specification. Further, as suggested in the specification the rule table can be implementation choice, making C2 active at time T5 instead of time T4 (Fig.3–4). This further negates the claim because active output signal would not be changing in response to active input signal in current context (A2) but would be changing in response to other input signal (B2) not under the consideration in present context.

Similar reasoning applies to the AND operator rules (Table 2), where the first combination (Output value=0, Active input value=0, other input value=0) makes the active input a required input to be true. Switching active input from 1 to 0 may or may not change the "output value" independent of other active input and depends on "other input value". Hence (1,0) (active input value, other input value) transition to (0,0) will not cause the change in the value of "output value" but a (1,1) transition will cause the change in value if "output value" from 1 to 0. Hence the exemplary rule table is not enabling in the light of the provided claim and contradicts the claimed subject matter.

Claim Interpretation

3. Regarding Claim 1

Claim 1 recites:

> an active output signal being any output signal of any component in the circuit connection graph that ***obtains a state*** between the start time and the stop time in response to a state change of the at least a start signal according to an execution path of the HDL code;"

The phrase "output signal ... obtains a state" is understood as "output signal changing the state" based on the state change of the start signal (active input signal). Claim 1 rejection based on 35 USC 112 ¶1 above is based on the interpretation that the output signal state is changed based on the change in input (start) signal within the start and stop time specified.

4. Regarding Claim 6

Claim 6 recites:

> "The method of claim 5 wherein the at least an instruction node of the connected component includes an entry-point node that must be satisfied before other instruction nodes of the connected component are subsequently executed, and the simulation results at the execution time satisfy the entry-point node."

This claim inherits from claim 5. In claim 5 "instruction node" is defined as a "logical instruction step". Claim 6 discloses "instruction node of the connected component". Examiner is unclear what is meant by "logical instruction step of the connected component" as defined. If the "logical instruction step" is understood as for example as AND operation then the connected component is understood as an AND gate. Further the claim discloses, "satisfying" the "entry point node". As best understood by examiner this means input is changing at the entry point node for the connected component.

5. Regarding Claim 11

Claim 11 recites "differentiated active component" and specification does not disclose any definition for any such component. As best understood by examiner these are "active components" that are "different" from other active components, such as a selected active components.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-13, 15-25, 27-28, 30-70, 72-82, 84-85, 87-101 and 102-114 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Application No. 09/829535 filed by Yu-Chin Hsu et al (Hsu hereafter).**

Regarding Claim 1

Hsu teaches, An active path extraction method for hardware description language (HDL) code in a computer system, the computer system comprising user input equipment for accepting input from a user, and user output equipment for providing output to the user, the HDL code being used to represent an electronic circuit having a plurality of components, each component having at least an input signal and an output signal (Hsu: [0054]-[0056]; Fig1-6; [0051]).

Hsu teaches utilizing the user input equipment to obtain at least a start signal from the user, the at least a start signal being an output signal (Hsu: [0051]) or an input signal (Hsu: [0009][0040], Fig.4).

Hsu teaches utilizing the user input equipment to obtain at least a stop signal from the user, the at least a stop signal being an output signal or an input signal (Hsu: [0009][0040]-[0043] & [0053], Fig.4).

Hsu teaches utilizing the user input equipment to obtain a start time and a stop time (Hsu: [0009] & Fig.4, [0053] Lines 1-3).

Hsu teaches obtaining simulation results of the electronic circuit from a simulator, as waveform, that utilizes the HDL code, the simulation results having state changes of the output signals and the input signals (Hsu: [0009] & Fig 4, [0034] [0035]).

Hsu teaches parsing the HDL code to obtain a circuit connection graph, as netlist, between the at least a start signal and the at least a stop signal, as component in put and out put of R1 and R6 respectively; the connection graph comprising components (registers, logic gates etc), input signals, and output signals that electrically connect the at least a start signal to the at least a stop signal (Hsu: [0033], Fig 1-4).

Hsu teaches utilizing the simulation results and the HDL code to determine which of the components in the circuit connection graph are active components, an active component being any component in the circuit connection graph having an active output signal, an active output signal being any output signal of any component in the circuit connection graph that obtains a state between the start time and the stop time in response to a state change of the at least a start signal according to an execution path of the HDL code (Hsu: at least in [0044], Fig.9-11).

Hsu teaches utilizing the user output equipment to provide the active components or the active output signals to the user as display of the active components (Hsu: Fig 11).

Regarding Claim 2

Hsu teaches user output equipment (e.g. computer display) is utilized to provide both the active components (Registers & combination logic) (Hsu: Fig 14) and the active output signals to the user (Hsu: Fig 14).

Regarding Claim 3

Hsu teaches forward search method for finding active components by iterating, as FAN_OUT method performed iteratively (Hsu: [0052]). Hsu teaches obtaining an active input signal (Hsu: [0051] Lines 9-10); utilizing the connection graph (as netlist) to obtain a connected component, the connected component having the active input signal as an input signal of the connected component (Hsu: [0059]); utilizing the HDL code and the simulation results to obtain the execution path (logged in the event list) of the connected component at an execution time that is between the start time and the stop time (Hsu: [0057] [0059])).

Hsu teaches and utilizing the execution path to determine if an output signal of the connected component is an active output signal of the connected component, wherein the output signal of the connected component is an active output signal of the connected component only if the output signal of the connected component obtains a state in response to a state change of the active input signal (Hsu: [0064]); wherein active output signal of the connected component is utilized as an active input signal in a subsequent iteration of the forward search method; wherein the first iteration of the forward search method utilizes the at least a start signal as the active input signal (Hsu: [0051][0052][0064]).

Regarding Claim 4

Hsu teaches utilizing the execution path to determine if the output signal is an active out put signal by obtaining the an equation that generates a value of the output signal of the connected component according to at least an input signal of the connected component, wherein if the active input signal is not within the equation, then the output signal of the connected component is not an active output signal of the connected component (Hsu: Fig.20, [0044][0059]); and parsing the equation to determine if the active input signal within the equation is a required signal for the value of the output signal of the connected component; wherein if the active input signal is a required signal, then the output signal of the connected component is an active output signal of the connected component. (Hsu: [0064][0065]).

Regarding Claim 5

Hsu teaches parsing the HDL code corresponding to the connected component to obtain at least an instruction node, each instruction node corresponding to a logical instruction step of the HDL code as a netlist (Hsu: [0004][0005]) and the associated logic; and iteratively substituting simulation results (as user selecting expanded Fan-out node and then clicking "FAN-OUT" button again) (Hsu: [0051]-[0053]), corresponding to a time on or after the execution time into the at least an instruction node according to the at least an instruction node to determine which instruction nodes of the connected component are executed at or after the execution time to obtain the value of the output signal of the connected component, wherein the execution path consists of executed instruction nodes (Hsu: [0007]-[0009], [0051]-[0053]). Hsu teaches that utilizing the execution path to obtain the equation that

generates the value of the output signal of the connected component comprises: linking logical statements derived from each instruction node in the execution path together by a logical AND operator to obtain a Boolean equation that generates the output value of the output signal of the connected component according to at least an input signal of the connected component as shown in with output R3 having at least an input signal connected component from R6 with AND operators (Hsu: Fig 15 & 16).

Regarding Claim 6

Hsu teaches an instruction node of the connected component (e.g. Fig.16: AND gate between time marker 10 & 20) includes an entry-point node (e.g. Fig.16: Register input from R6) that must be satisfied before other instruction nodes of the connected component are subsequently executed, and the simulation results at the execution time satisfy the entry-point node (Fig 15, R6 input is changing to AND Gate shown in the Fig 16).

Regarding Claim 7 & 8

Hsu teaches that execution time is a simulation time that is closest to the start time as starting the simulation from time 0 but the input execution happens at time 10 when the signal for Register R6 changes (Hsu: [0051]); and execution time is a simulation time that is closest to a state change of the at least a start signal, where input to register R6 is the start signal to the following AND gate (Hsu: [0051]).

Regarding Claim 9

Hsu teaches

> "active input signal has an associated local input time, and the active output signal of the connected component has an associated local output time that is the earliest simulation time on or after the local input time at which the output signal of the connected component obtains a state in response to a state change of the active input signal; wherein the local output time is utilized as a local input time in a subsequent iteration of the forward search method"

as local start time and local stop time as section of simulation for the start signal under observation, where the change in start signal starts a local start time and end of observation stops the local stop time (Hsu: Fig.16 shows time 10 as local start time and time 20 as local stop time for first iteration). The local stop time for the first iteration, time 20, becomes local start time for the next forward iteration and local stop time now is time 30.

Regarding Claim 10

Hsu teaches execution time is a simulation time on or after the local input time (Hsu: Fig.16) where execution time is time 10 after the simulation time.

Regarding Claim 11

As interpreted above in claim interpretation section, "differentiated active component" is a selected active component. Hsu teaches differentiated active component is provided to the user in a differentiated manner according to the local input time or the local output time of the differentiated active component on the display to select (Hsu: Fig.16, [0052]).

Regarding Claim 12

Hsu teaches required signals (signals that are changing at the instruction nodes, that change the output) of the active output signal of the differentiated active component

are further provided (Hsu: Fig.16 R6/S4 pair for AND gate between time 10 & time 20, S4/S2 pair AND between time 20 and 30 – R4 is not a required signal).

Regarding Claim 13

Hsu teaches values of the required signals at the local output time or the local input time are further provided (Hsu: Fig.16). Input R5 changing from 0 to 1 (0>1 convention used) at local input time of AND gate between time 20 and 30. Output S2 changing from 0 to 1 at local output time 30.

Regarding Claim 15

Hsu teaches an animated display of the active components or active signals according to the local input times or the local output times (Hsu: Fig.16).

Regarding Claim 16

Hsu teaches adding the connected component to an active component list if the output signal of the connected component is an active output signal as seen the by the registers and connected gates in Fig.16, where the all the active input and output signals & components are displayed and the list containing is generated from FAN_OUT LIST GEN module (Hsu: Fig 18). Further, Hsu teaches adding the output signal of the connected component to an active signal list if the output signal of the connected component is an active output signal as the all the signals that impact the FANOUT (Hsu: Fig 20; [0051][0052] [0059]). Further it is clear from Fig.11 that the active components and paths are clearly identified by the bolded connection between start signal and stop signal and non-active parts are only highlighted by the thin “fly-line”.

Regarding Claim 17

Hsu teaches backward search method for finding active components by iterating, as FAN_IN method performed iteratively (Hsu: [0040]- [0043]). Hsu teaches obtaining a start-point active output signal (Hsu: [0040] Lines 1-9); utilizing the connection graph to obtain a connected component, the connected component having the start-point active output signal as an output signal of the connected component [Hsu: [0040] Lines 10-11; [0048], Fig.12); utilizing the HDL code and the simulation results to obtain the execution path of the connected component at an execution time that is between the start time and the stop time (Hsu: [0041; Fig.12)]; and utilizing the execution path to determine if an input signal of the connected component is an active input signal of the connected component (Hsu: [0044] Fig 9), wherein the input signal of the connected component is an active input signal of the connected component only if the start-point active output signal obtains a state in response to a state change of the input signal of the connected component; wherein the active input signal of the connected component is utilized as a start-point active output signal in a subsequent iteration of the backward search method (Hsu: [0042]; Fig.5); wherein the first iteration of the backward search method utilizes the at least a stop signal as the start-point active output signal (Hsu: Fig.5-8).

Regarding Claim 18

Hsu teaches execution time is a simulation time at which the start-point active output signal undergoes a state change (Hsu: Fig.6 R1 changing from 0 to 1).

Regarding Claim 19

Hsu teaches utilizing the execution path to obtain an equation that generates the value of the start-point active output signal according to signals within the execution path (Hsu: [0058]; Fig.19), wherein if the input signal of the connected component is within the equation, then the input signal of the connected component is an active input signal of the connected component.

Hsu teaches parsing the equation to determine if the input signal of the connected component within the equation is a required signal for the value of the start-point active output signal [0044]; wherein if the input signal of the connected component is a required signal, then the input signal of the connected component is an active input signal of the connected component.

Regarding Claim 20

Hsu teaches parsing the HDL code corresponding to the connected component to obtain at least an instruction node, each instruction node corresponding to a logical instruction step of the HDL code as a netlist (Hsu: [0004][0005]); and utilizing the simulation results corresponding to a time on or before the execution time and the at least an instruction node to back-trace the at least an instruction node to determine which instruction nodes of the connected component are executed on or before the execution time to obtain the value of the start-point active output signal (Hsu: [0042][0058]), wherein the execution path consists of all instruction nodes executed to generate the value of the start-point active output signal at the execution time; and utilizing the execution path to obtain the equation that generates the value of the start-point active output signal comprises: linking logical statements derived from

each instruction node in the execution path together by a logical AND operator to obtain a Boolean equation that generates the value of the start-point active output signal according to signals in the logical statements (Hsu: at least in Fig 6-11; Fig 19; [0058]).

Regarding Claim 21

Hsu teaches start-point active output signal has an associated local output time, and the active input signal of the connected component has an associated local input time that is the latest simulation time on or before the local output time at which the active input signal of the connected component undergoes a state change; wherein the local input time is utilized as a local output time in a subsequent iteration of the backward search method (Hsu: Fig.11). Further, this limitation for the backward traversal is very similar to the forward traversal as disclosed on claim 9 and further rejected for the same reason.

Regarding Claim 22

Hsu teaches the execution time is a simulation time on or before the local output time (Hsu: Fig.11).

Regarding Claim 23

Hsu teaches differentiated active component is provided to the user in a differentiated manner according to the local input time or the local output time of the differentiated active component on the display to select (Hsu: Fig.12, [0047]).

Regarding Claim 24

Hsu teaches required signals (signals that are changing at the instruction nodes, that change the output) of the active output signal of the differentiated active component are further provided (Hsu: Fig.12, R2 is the required signal for the active output signal R1 for the differentiated active component AND gate).

Regarding Claim 25

Hsu teaches values of the required signals at the local output time or the local input time are further provided (Hsu: Fig.12).

Regarding Claim 27

Hue teaches an animated display of the active components (Hsu: Fig.12) or active signals (Hsu: Fig.11 Bolded paths Between R1, R2, R3) according to the local input times (Hsu: Fig.11 time 90) or the local output times (Hsu: Fig.11 time 80).

Regarding Claim 28

Hsu teaches adding the connected component to an active component list, and adding the input signal of the connected component to an active signal list if the input signal of the connected component is an active input signal of the connected component (Hsu: Fig.18 Element 144, 146 & 142 and Fig.12 & [0047] associate the active components to the selected active signals).

Regarding Claim 30

Method claim 30 recites similar limitations as claim 3 and its preceding independent parent claim and is rejected for the same reasons as claim 3.

Regarding Claim 31

Hsu teaches user output equipment (e.g. computer display) is utilized to provide both the active components (Registers & combination logic) (Hsu: Fig 14) and the active output signals to the user (Hsu: Fig 14).

Regarding Claim 32

Method claim 32 recites similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 33

Method claim 33 recites similar limitations as claim 5 and is rejected for the same reasons as claim 5.

Regarding Claim 34

Method claim 34 recites similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 35 & 36

Method claims 35 & 36 recite similar limitations as claim 7 & 8 respectively and are rejected for the same reasons as claim 7 & 8.

Regarding Claim 37

Method claim 37 recites similar limitations as claim 9 and is rejected for the same reasons as claim 9.

Regarding Claim 38

Method claim 38 recites similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 39

Method claim 39 recites similar limitations as claim 11 and is rejected for the same reasons as claim 11.

Regarding Claim 40

Method claim 40 recites similar limitations as claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 41

Method claim 41 recites similar limitations as claim 13 and is rejected for the same reasons as claim 13.

Regarding Claim 42

Method claim 42 recites similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claim 43

Method claim 43 recites similar limitations as claim 15 and is rejected for the same reasons as claim 15.

Regarding Claim 44

Method claim 44 recites similar limitations as claim 16 and is rejected for the same reasons as claim 16.

Regarding Claim 45

Method claim 45 recites similar limitations as claim 17 & its preceding independent parent claim 1 and is rejected for the same reasons as claim 17.

Regarding Claim 46

Method claim 46 recites similar limitations as claim 2 & its preceding independent parent claim 1 and is rejected for the same reasons as claim 2.

Regarding Claim 47

Method claim 47 recites similar limitations as claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 48

Method claim 48 recites similar limitations as claim 19 and is rejected for the same reasons as claim 19.

Regarding Claim 49

Method claim 49 recites similar limitations as claim 20 and is rejected for the same reasons as claim 20.

Regarding Claim 50

Method claim 50 recites similar limitations as claim 21 and is rejected for the same reasons as claim 21.

Regarding Claim 51

Method claim 51 recites similar limitations as claim 22 and is rejected for the same reasons as claim 22.

Regarding Claim 52

Method claim 52 recites similar limitations as claim 23 and is rejected for the same reasons as claim 23.

Regarding Claim 53

Method claim 53 recites similar limitations as claim 24 and is rejected for the same reasons as claim 24.

Regarding Claim 54

Method claim 54 recites similar limitations as claim 25 and is rejected for the same reasons as claim 25.

Regarding Claim 55

Method claim 55 recites similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claim 56

Method claim 56 recites similar limitations as claim 27 and is rejected for the same reasons as claim 27.

Regarding Claim 57

Method claim 57 recites similar limitations as claim 28 and is rejected for the same reasons as claim 28.

Regarding Claims 58-70

Hsu teaches a system where the disclosed input equipment (mouse/pointer device) (Hsu: [0040]), output equipment (display/display controller) (Hsu:[0056]), CPU and memory are either anticipated or inherent in the system taught by Hsu. Computer system claims 58-70 recite similar limitations as claims 1-13 and are rejected for the same reasons as claims 1-13 respectively.

Regarding Claims 72-82

Computer system claims 72-82 recite similar limitations as claim 15-25 and are rejected for the same reasons as claim 15-25 respectively.

Regarding Claims 84-85

Computer system claims 84-85 recite similar limitations as claim 27-28 and are rejected for the same reasons as claim 27-28 respectively.

Regarding Claims 87-101

Hsu teaches a system where the disclosed input equipment (mouse/pointer device) (Hsu: [0040]), output equipment (display/display controller) (Hsu:[0056]), CPU and memory are either anticipated or inherent in the system taught by Hsu. Computer system claims 87-101 recite similar limitations as claims 30-44 and are rejected for the same reasons as claims 30-44 respectively.

Regarding Claims 102-114

Hsu teaches a system where the disclosed input equipment (mouse/pointer device) (Hsu: [0040]), output equipment (display/display controller) (Hsu:[0056]), CPU and memory are either anticipated or inherent in the system taught by Hsu. Computer system claims 10-114 recite similar limitations as claims 45-57 and are rejected for the same reasons as claims 45-57 respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claim 14, 26, 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over obvious, in view of U.S. Application No. 09/829535 filed by Yu-Chin Hsu et al (Hsu hereafter).**

Regarding Claim 14

Hsu teaches active path extraction through forward traversal (FANOUT) as disclosed in claim 11 and preceding parent claims.

Hsu does not teach obtaining breakpoint from the user explicitly to select the active component at that time.

Examiner takes official notice that providing breakpoint to halt simulation is known in the art. Further, using breakpoint in post simulation analysis is equivalent to "go to time step" command known in the art and would be obvious to one skilled in the art of simulation at the time this invention was made.

Regarding Claim 26

Method claim 26 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claim 71

Computer system claim 71 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claim 83

Computer system claim 83 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

3. **Claims 29 and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Application No. 09/829535 filed by Yu-Chin Hsu et al (Hsu hereafter), in view of IEEE article "An Efficient Parallel Critical Path Algorithm" by Li-Ren Liu (Liu hereafter).**

Regarding Claim 29

Hsu teaches forward and backward traversals with iterations (Hsu: [0012][0044] [0047]) to determine the active paths and use "SHOW LOGIC feature to identify the active components between the input active signal and output active signals.

Hsu does not teach intersecting the first set (from forward traversal) of active components with the second set (from backward traversal) of active components to obtain active components.

Liu teaches forward traversal and backward traversal (Liu: Pg.911 Col.2). Further Liu teaches sensitizing active path by performing an intersection of the two traversals (Liu: Pg.913-914, Rule 3-5; Pg. 913 Col.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Liu to Hsu. The motivation to combine would have been that active path extraction (through backward & forward path traversal) is performed to determine the most critical path in terms of it delays (Yen[1]: Abstract). Liu teaches an efficient parallel critical path extraction through backward & forward traversal and combining the two derive traversals all the active components in a path are presented, thus giving the optimum result.

[1] "Efficient Algorithm for Extraction the K Most Critical Paths in Timing Analysis" by Steve H.C. Yen et al (ACM 1989)

Regarding Claim 86

Computer system claim 86 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Conclusion

4. All claims are rejected.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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